



FIG. 2A

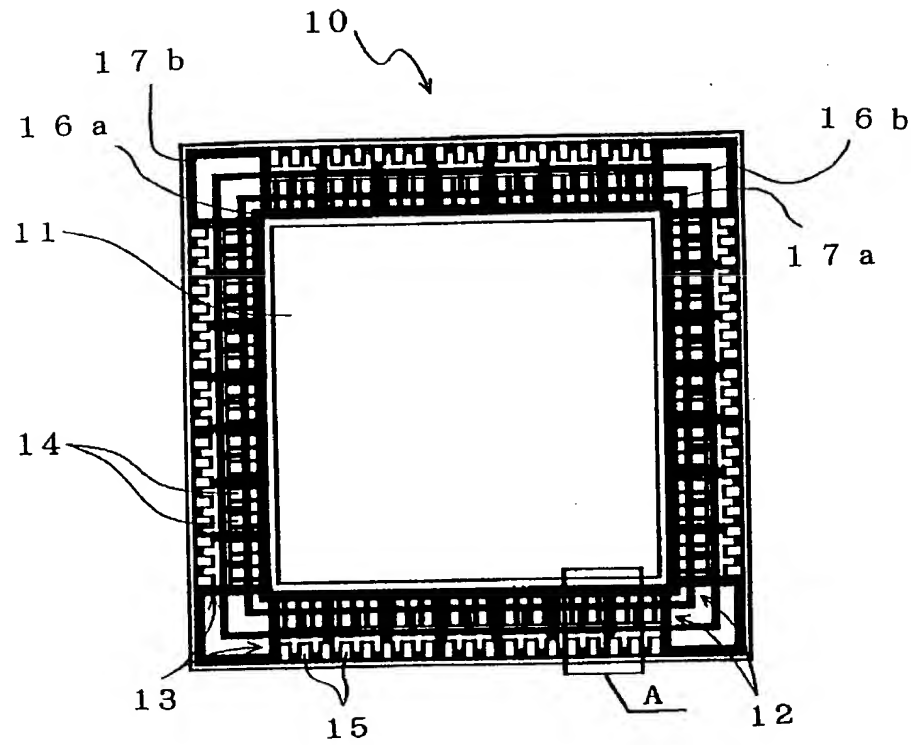


FIG. 2B

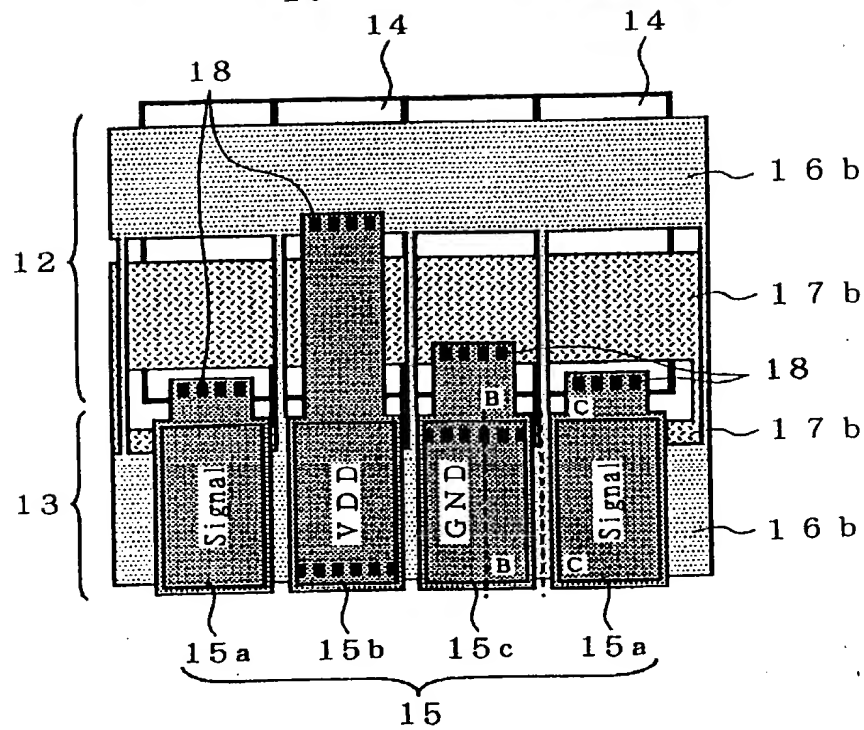


FIG.3A

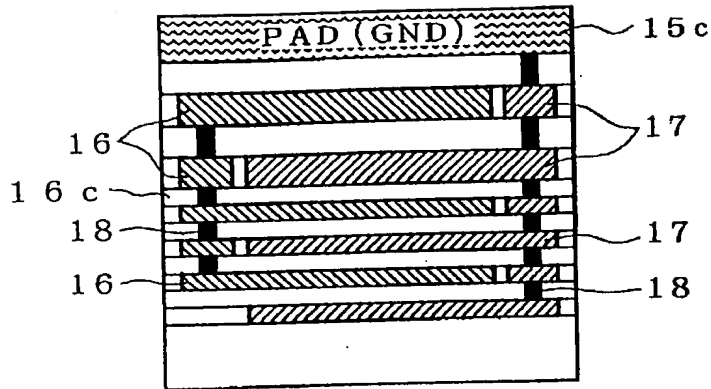
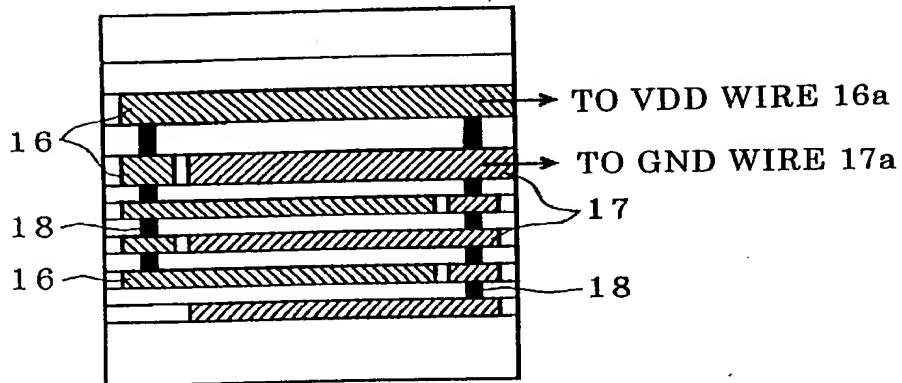
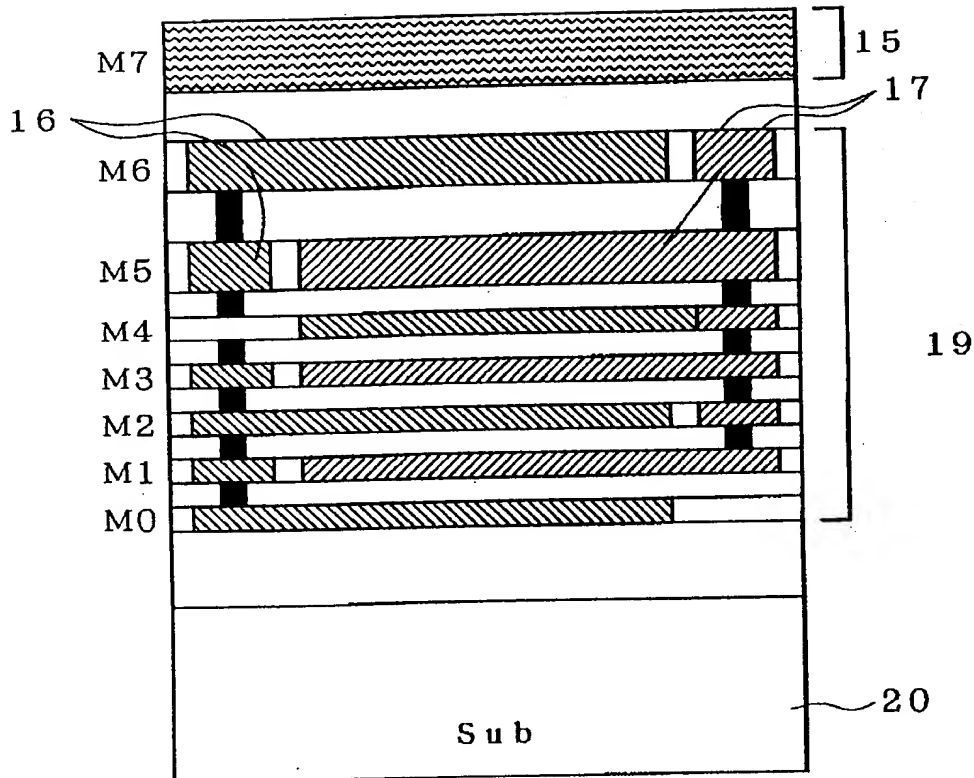


FIG.3B



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FIG. 4



The diagram illustrates a cross-section of a semiconductor device. A stack of memory cells, labeled M0 through M7, is positioned above a peripheral circuit region. Each memory cell layer (M0-M7) consists of alternating horizontal segments with different patterns (dots, diagonal lines, and white). A vertical bracket on the right side of the memory stack is labeled 21. Below the memory stack, the peripheral circuit region (labeled 22) contains several components: two P-channel transistors (Pch Tr) and two N-channel transistors (Nch Tr). The Pch Trs have P+ regions in their gates, while the Nch Trs have N+ regions. These transistors are connected to a common source line (Sub) at the bottom. A vertical bracket on the right side of the peripheral circuit is labeled 22. The entire device is built on a substrate (Sub). A label 22a points to the peripheral circuit region, and a label 22b points to the substrate. A label 20 is located at the bottom right corner.

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FIG.7A

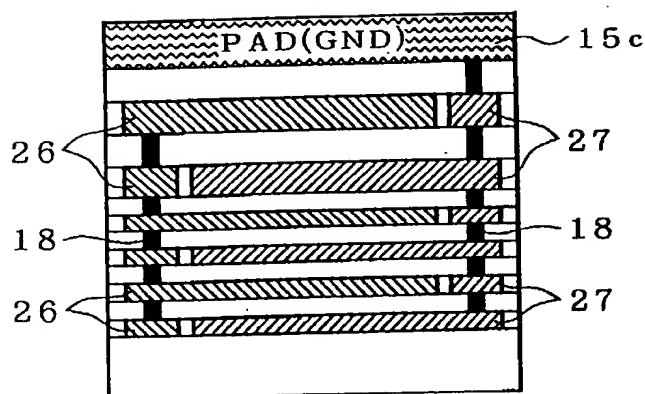


FIG.7B

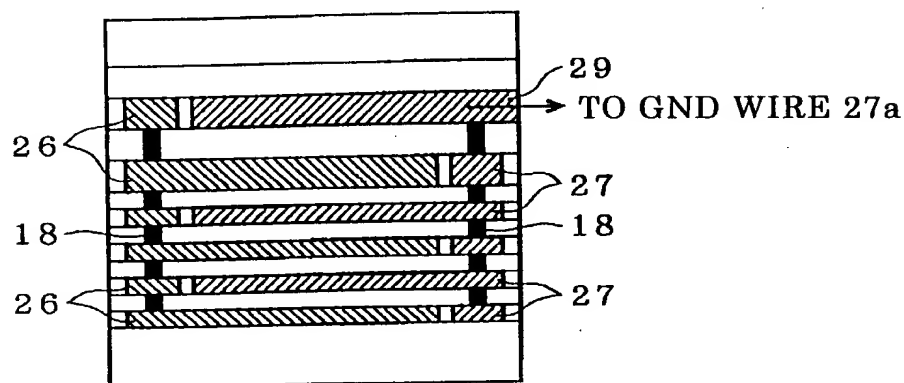


FIG.7C

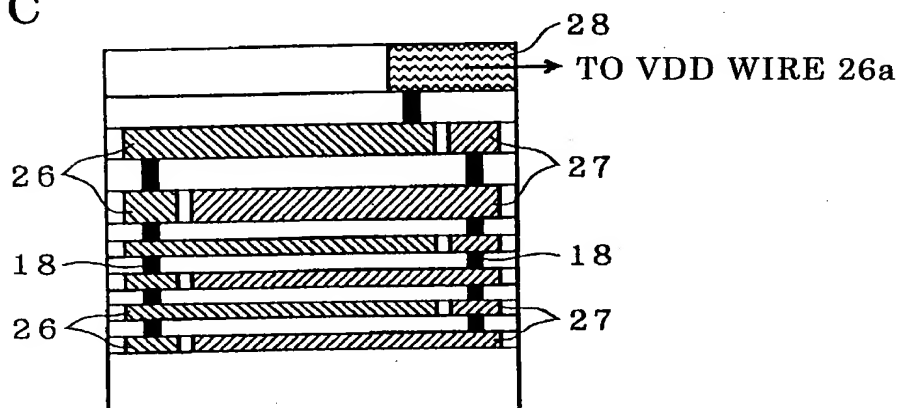
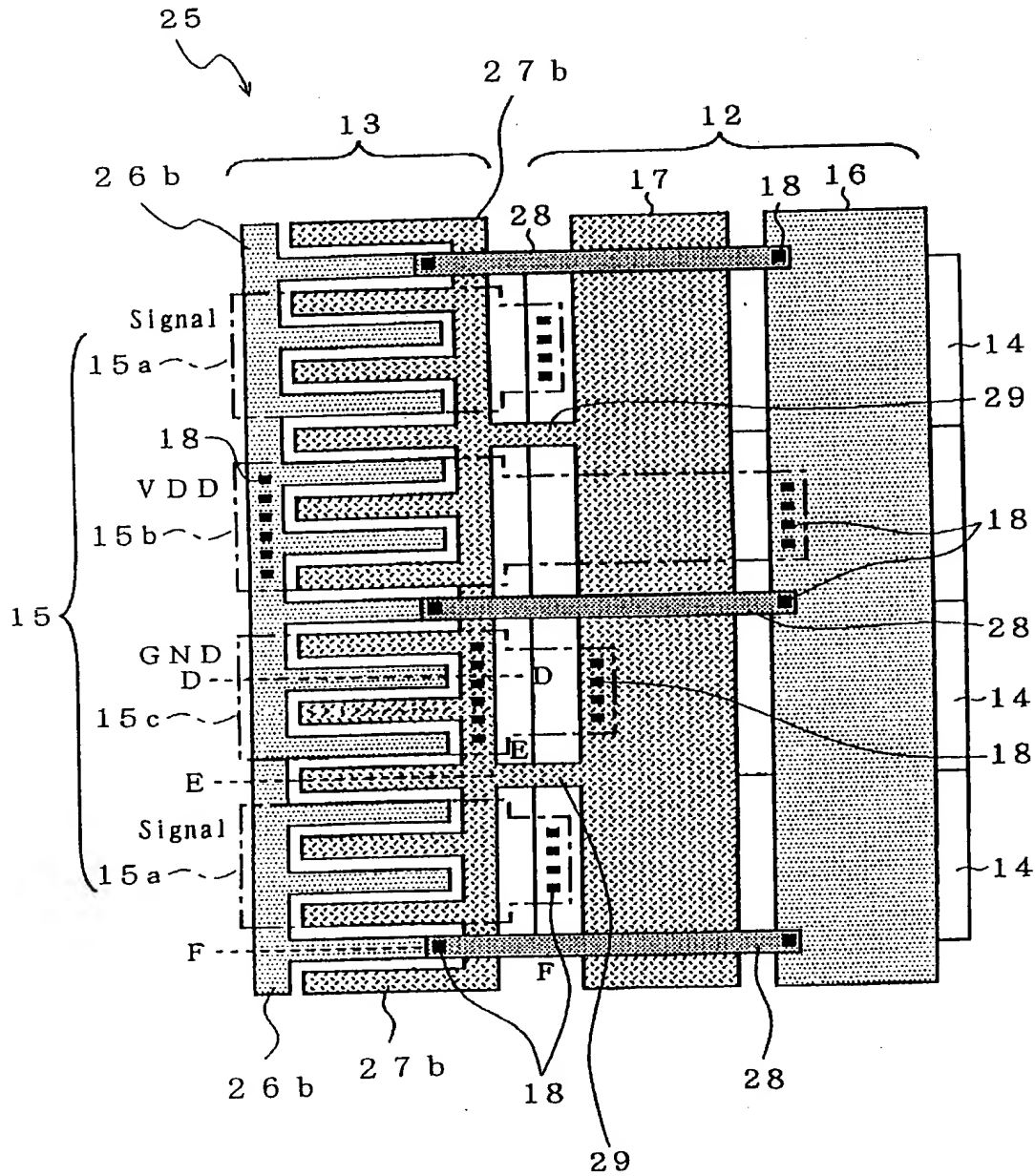


FIG.6



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FIG.8A

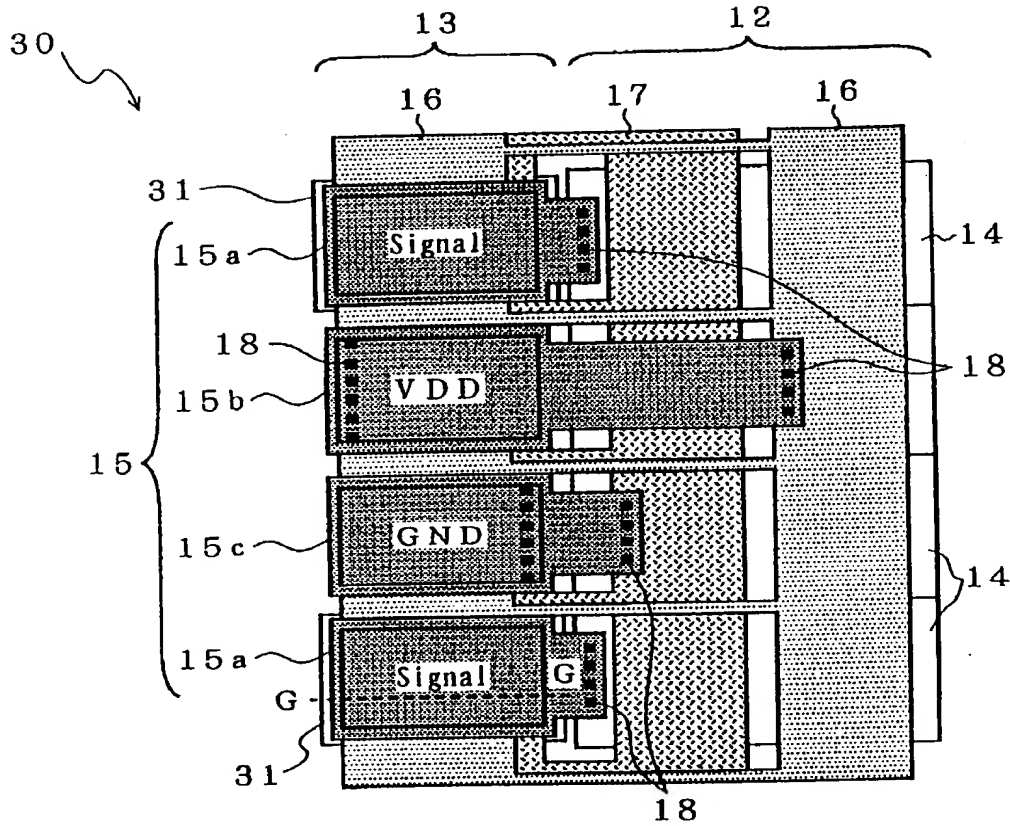
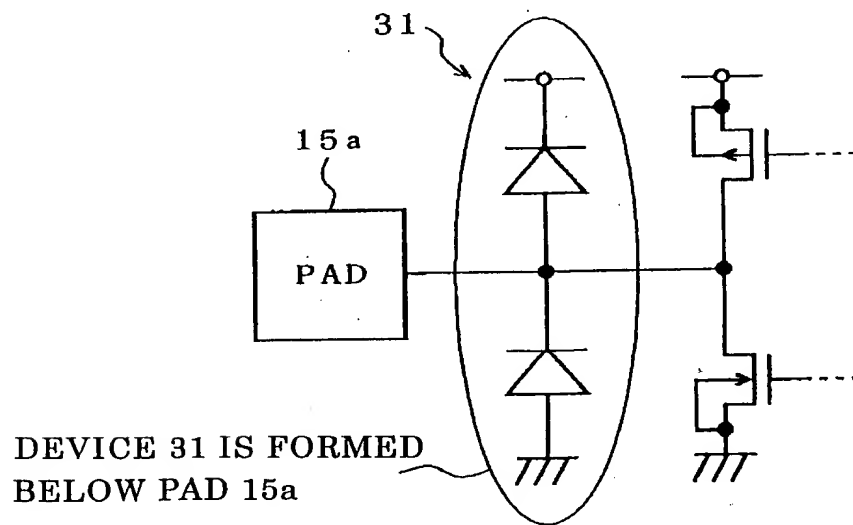


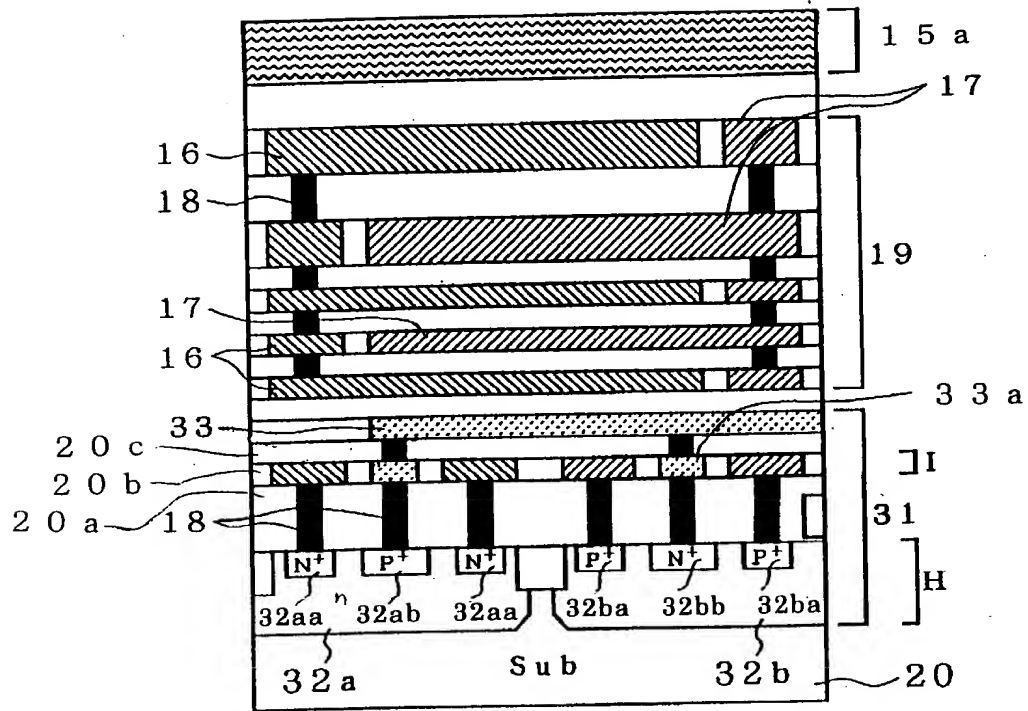
FIG.8B





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FIG.9



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FIG.10A

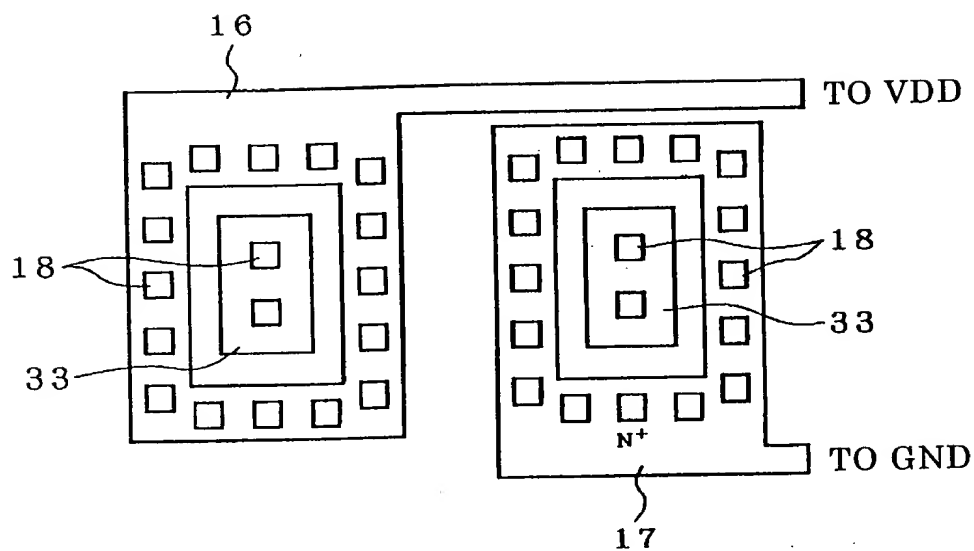


FIG.10B

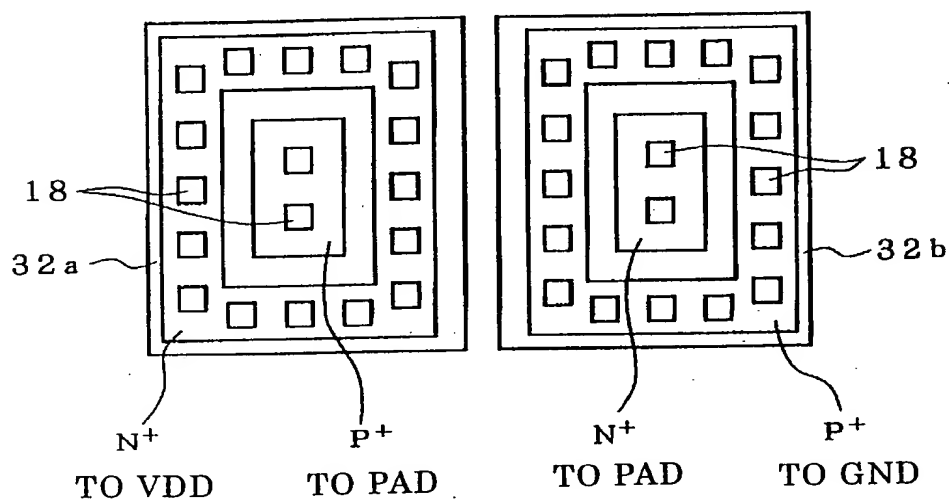
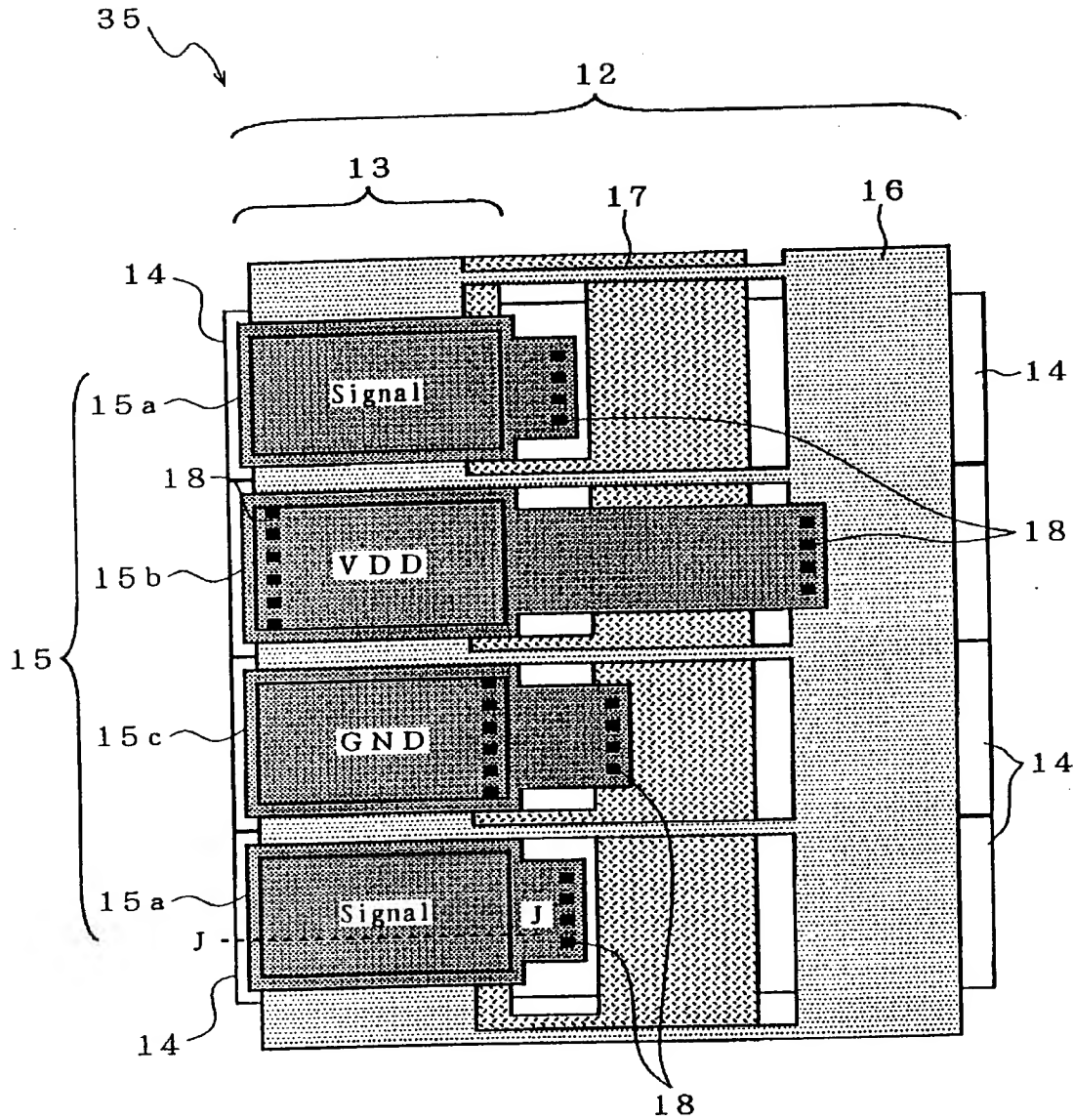


FIG.11



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FIG.12

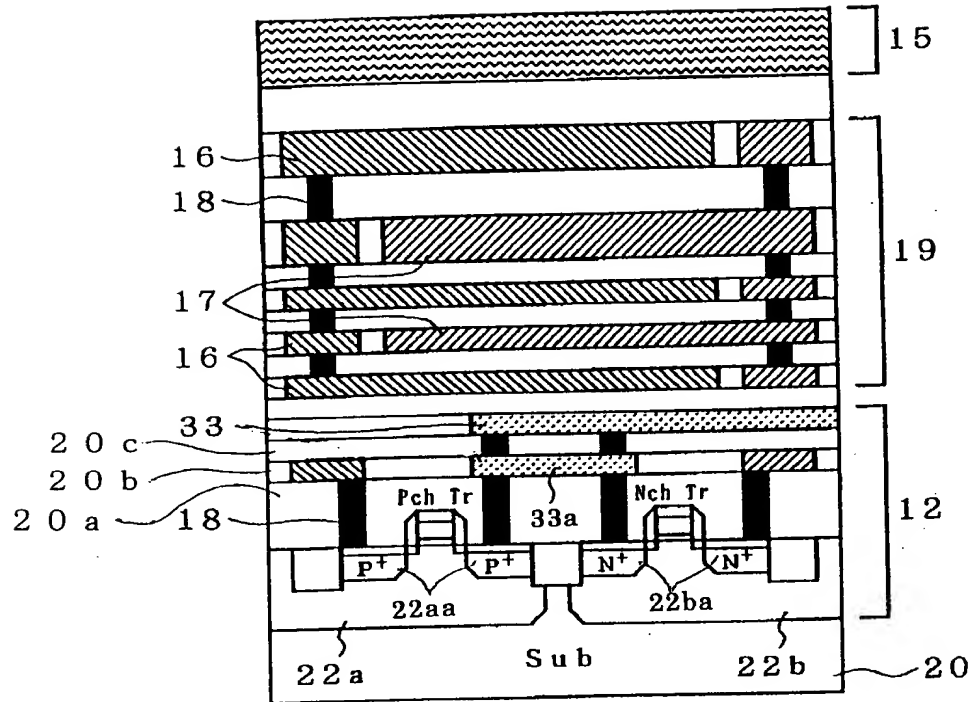


FIG.13

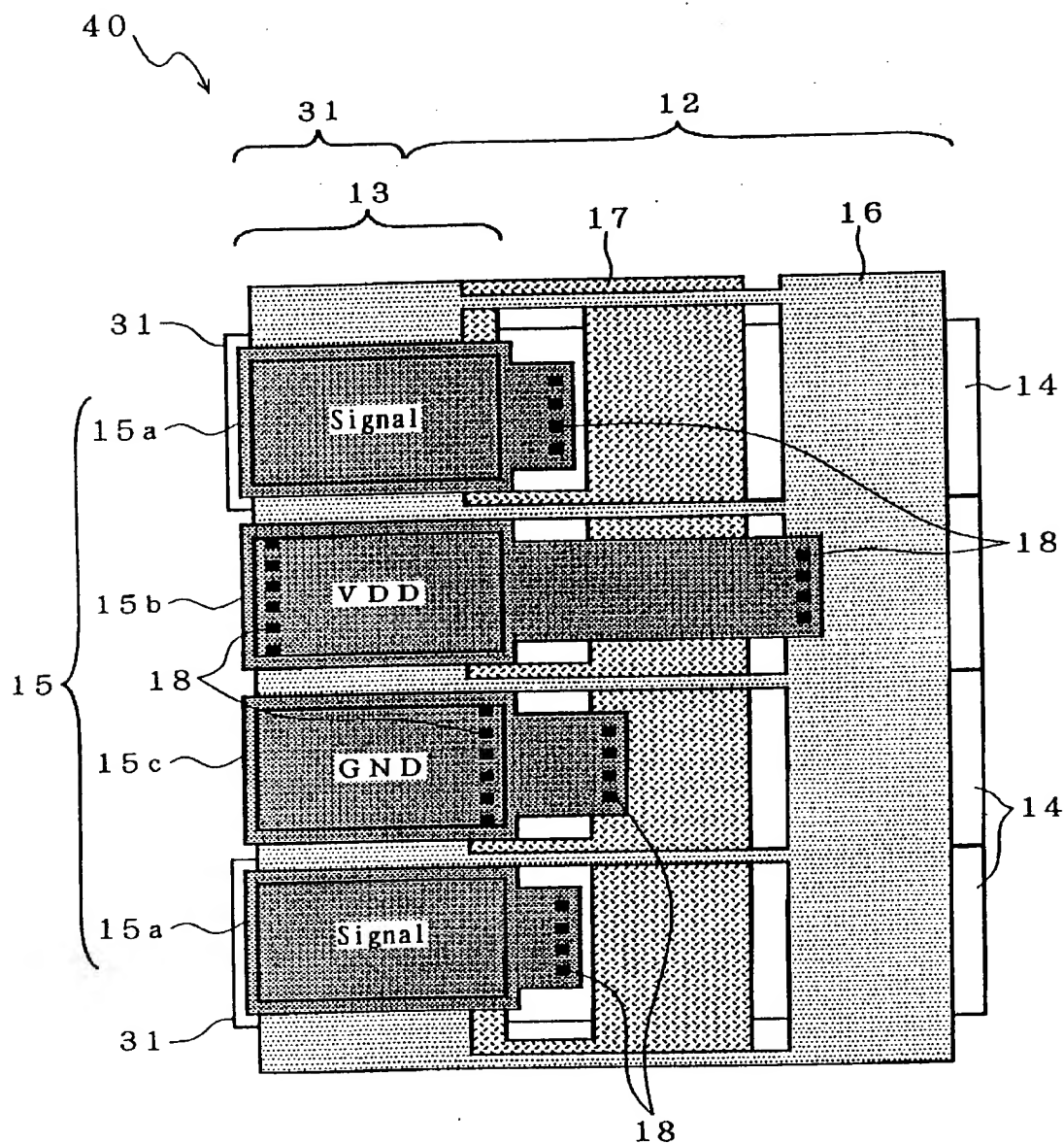


FIG. 14

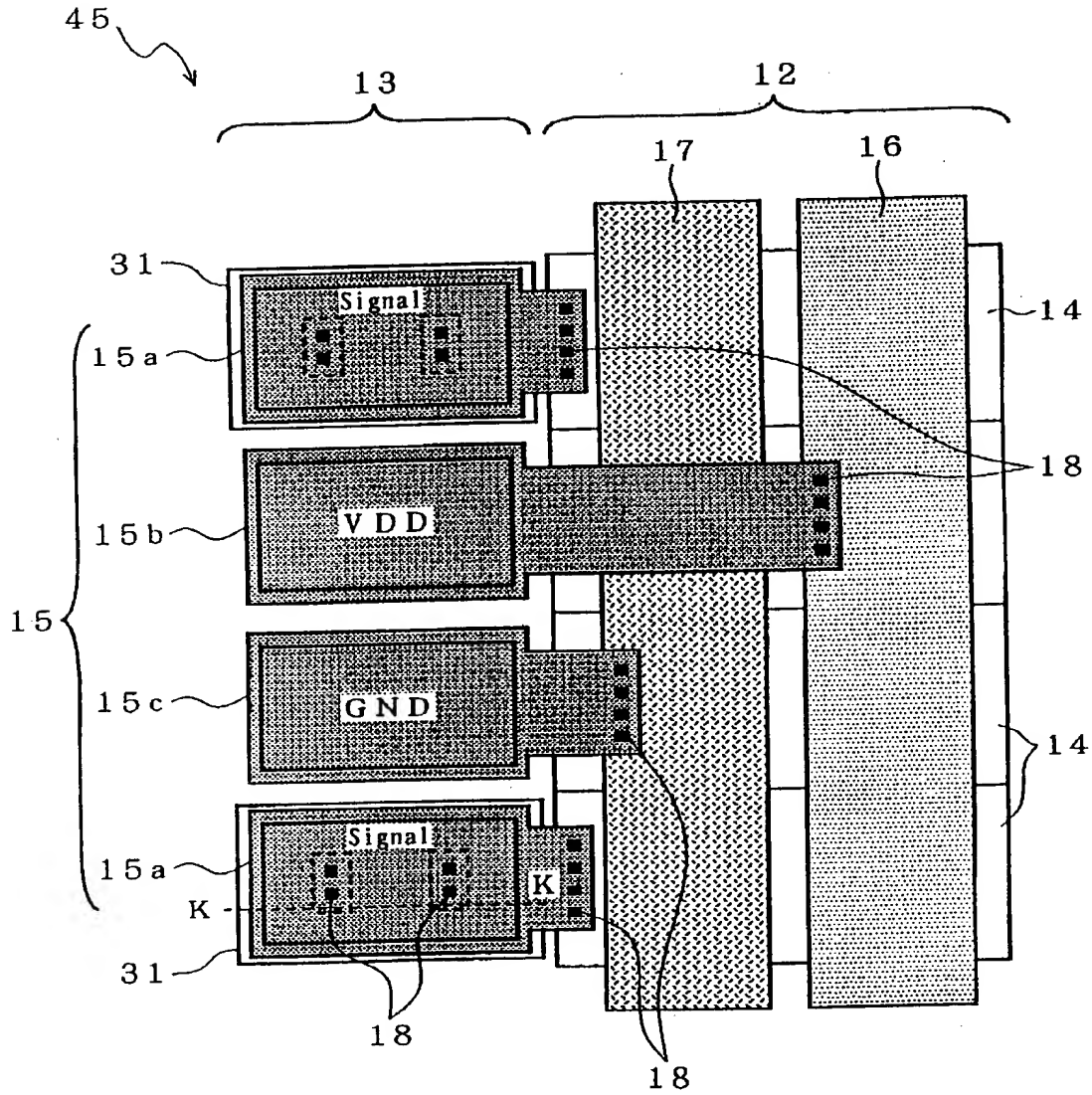


FIG. 15

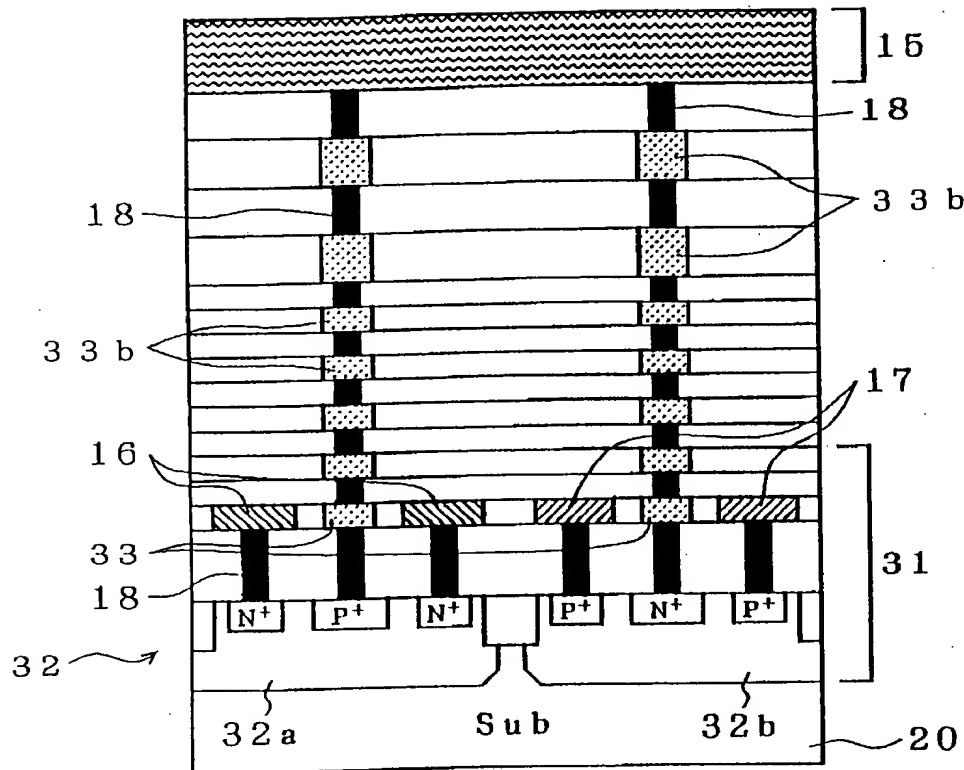


FIG. 16

